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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,834	03/04/2004	Peer Gil Schmitt	003921.00148	3853

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SUITE 1100  
WASHINGTON, DC 20001

EXAMINER
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LE, THONG QUOC

ART UNIT	PAPER NUMBER
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2827

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

3m

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/791,834	SCHMITT, PEER GIL	
	<b>Examiner</b>	<b>Art Unit</b>	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
       Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
       Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____.  |

**DETAILED ACTION**

1. Claims 1-9 are presented for examination.

***Information Disclosure Statement***

2. This office acknowledges receipt of the following items from the Applicant:  
Information Disclosure Statement (IDS) filed on 03/04/2004.
3. Information disclosed and list on PTO 1449 was considered.

***Specification***

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Kablanian (U.S. Patent No. 6,104,663).

Regarding claim 1, Kablanian discloses a memory device (Figure 5) , comprising:

a plurality of addressable memory cells (502, 504), each memory cell configured to store a first bit and a second bit (ABSTRACT), each memory cell including:

a first storage circuit configured to store the first bit (ABSTRACT); and

a second storage circuit (ABSTRACT) configured to store the second bit and coupled to the first storage circuit, and further configured to deactivate the first storage circuit based on the second bit (Column 4, lines 7-26, Column 7, lines 43-67, Column 8, lines 1-7).

Regarding claims 2-3, Kablanian discloses first bit line coupled to at least one of the memory cells, wherein the first storage circuit (Figure 5, 502) of the at least one memory cell includes: an enable node and a first output node, wherein the first storage circuit has either a high or low impedance at the first output node depending upon a logical value of the enable node, the first bit line selectively receiving a logical value of the first output node, and wherein the second storage circuit (Figure 5, 504) of the at least one memory cell includes: a second output node configured to control the enable node, the first bit line selectively receiving a logical value of the second output node (Column 4, lines 6-26, Column 5, lines 25-63), and including a second bit line coupled to the at least one memory cell, wherein the first storage circuit of the at least one memory cell includes a third output node, wherein the first storage circuit has either a high or low impedance at the third output node depending upon a logical value of the enable node, the third output node having a logic value opposite the first output node when the first storage circuit has a low impedance at the first and third output nodes, the second bit line selectively receiving a logical value of the third output node, and wherein the

second storage circuit of the at least one memory cell includes: a fourth output node having a value opposite the second output node, the second bit line selectively receiving a logical value of the fourth output node (Figure 5, Column 6, lines 52-67, column 8, lines 1-42).

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Hobson (U.S. Patent No. 6,804,143).

Regarding claim 1, Hobson discloses a memory device (Figure 10) , comprising:  
a plurality of addressable memory cells (50, 48), each memory cell configured to store a first bit and a second bit (Column 6, lines 25-40), each memory cell including:  
a first storage circuit configured to store the first bit ; and a second storage circuit (Figure 10, 50,48) configured to store the second bit and coupled to the first storage circuit, and further configured to deactivate the first storage circuit based on the second bit (Column 6 lines 25-67).

Regarding claims 2-5, Hobson discloses first bit line coupled to at least one of the memory cells, wherein the first storage circuit (Figure 10, 50) of the at least one memory cell includes: an enable node and a first output node, wherein the first storage circuit has either a high or low impedance at the first output node depending upon a logical value of the enable node, the first bit line selectively receiving a logical value of the first output node, and wherein the second storage circuit (Figure 10, 48) of the at least one memory cell includes: a second output node configured to control the enable node, the first bit line selectively receiving a logical value of the second output node (Column 6, lines 25-67, and including a second bit line coupled to the at least one memory cell, wherein the first storage circuit of the at least one memory cell includes a third output node, wherein the first storage circuit has either a high or low impedance at the third output node depending upon a logical value of the enable node, the third output node having a logic value opposite the first output node when the first storage circuit has a low impedance at the first and third output nodes, the second bit line selectively receiving a logical value of the third output node, and wherein the second storage circuit of the at least one memory cell includes: a fourth output node having a value opposite the second output node, the second bit line selectively receiving a logical value of the fourth output node (Figure 10, Column 5, lines 30-67), and wherein each first storage circuit (50) includes: a first inverter having an input, an output, and an output enable; a second inverter having an input, an output, and an output enable, the first and second inverters forming a first latch (Figure 10) ; and a first transistor (Figure 10) having a source and drain coupled between the output enables of the first and

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second inverters and a fixed potential (Figure 10), and a gate coupled to the second storage circuit (Figure 10), and wherein each second storage circuit (48) includes a second latch, the gate of the first transistor being coupled to a node of the second latch (Figure 10), a bit line selectively receiving a logical value of the node.

Regarding claims 6-9, Hobson discloses an apparatus (Figure 10), comprising: a plurality of dual-bit memory cells (50, 48), each memory cell including: a first storage circuit configured to store a first bit, and a second storage circuit configured to store a second bit; a first plurality of word lines (Figure 2, WL, Column 1, lines 64-67, column 5, lines 15-30) each controlling one of the first storage circuits; and a second plurality of word lines (Figure 2, WL, Column 1, lines 64-67, Column 5, lines 15-30) each controlling one of the second storage circuits, wherein the first storage circuit includes a transistor having a gate, the gate coupled to the second storage circuit so as to receive a value of the second bit, and wherein the first storage circuit includes a flip flop that stores the first bit and that has a control node, the transistor further coupled between the control node and a fixed potential, and wherein the second storage circuit includes a flip flop that stores the second bit at a storage node, the gate of the transistor being coupled to the storage node, and further including a bit line pair each coupled to one of the memory cells, each bit line pair coupled to logic that combines the respective bit line pair into a single logical value (Figure 10, Column 6, lines 25-67).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le  
Primary Examiner  
Art Unit 2827

**THONG LE**  
**PRIMARY EXAMINER**